What is claimed is:

1. A voltage amplification circuit comprising:

a first inverting amplifier placed in a first stage;

a second inverting amplifier placed in a second stage, said second inverting amplifier being DC-coupled to said first inverting amplifier; and

wherein an amplifying operation starting input voltage in said first inverting amplifier is set to be lower than an amplifying operation starting input voltage in said second inverting amplifier.

2. The voltage amplification circuit according to Claim 1, further comprising a clamping circuit to feed a clamping voltage to an input terminal for said first inverting amplifier and wherein a transistor placed on a load side making up said clamping circuit has substantially a same threshold value as a driver transistor in said second inverting amplifier.

3. A voltage amplification circuit comprising:

a first inverting amplifier placed in a first stage;

a second inverting amplifier placed in a second stage, said second inverting amplifier being DC-coupled to said first inverting amplifier;

wherein said first inverting amplifier comprises a first transistor with a drain and a gate of which are both connected to a terminal for a first potential and a second transistor with a gate of which is connected to an input node and with a source of which is connected to a terminal for a second potential, in

which a source of said first transistor is connected to a drain of said second transistor, an output of said first inverting amplifier being placed between said source of said first transistor and said drain of said second transistor;

wherein a second inverting amplifier comprises a third transistor with a drain and gate of which is connected to a terminal for said first potential and a fourth transistor with a gate of which is connected to a terminal for an output from said first inverting amplifier and with a source of which is connected to a terminal for said second potential, in which a source of said third transistor is connected to a drain of said fourth transistor, an output of said second inverting amplifier being placed between said source of said third transistor and said drain of said fourth transistor; and

wherein a threshold value of said fourth transistor is larger than a threshold value of said second transistor.

4. The voltage amplification circuit according to Claim 3, further comprising a clamping circuit to output a clamping voltage to a clamping node which has sixth and eighth transistors with drains and gates of which are connected commonly to a terminal for said first potential and seventh and ninth transistors with drains and gates of which are connected to sources of said sixth and eighth transistors and with sources of which are connected commonly to a terminal for said second potential and wherein said sources of said sixth and eighth transistors and said gates and said drains of said seventh and ninth transistors are connected to said clamp node and wherein said clamping circuit further has a fifth transistor with a gate of which is connected to a control

signal terminal and with a drain or with a source of which is connected to an input node of said first inverting amplifier and with a source or with a drain of which is connected to said clamping node and wherein threshold values of said fourth and eighth transistors are substantially same.

5. The voltage amplification circuit according to Claim 3, wherein a non-inverting amplifier is added which has a tenth transistor with a drain of which is connected to a terminal for said first potential and with a gate of which is connected to an output terminal for said second inverting amplifier and an eleventh transistor with a gate of which is connected to an output terminal for said first inverting amplifier and with a source of which is connected to a terminal for said second potential and wherein a source of said tenth transistor is connected to a drain of said eleventh transistor and a voltage is output therefrom.

6. The voltage amplification circuit according to Claim 3, wherein a transistor for controlling supply of a source voltage is connected to a connecting point to a terminal for said first potential wherein, while a control signal is active, said first potential is applied to said clamping circuit and while said control signal is inactive, said first potential is applied to an amplifying section.

7. The voltage amplification circuit according to Claim 4, wherein a non-inverting amplifier is added which has a tenth transistor with a drain of which is connected to a terminal for said first potential and with a gate of which is connected to an

output terminal for said second inverting amplifier and an eleventh transistor with a gate of which is connected to an output terminal for said first inverting amplifier and with a source of which is connected to a terminal for said second potential and wherein a source of said tenth transistor is connected to a drain of said eleventh transistor and a voltage is output therefrom.

8. The voltage amplification circuit according to Claim 4, wherein a transistor for controlling supply of a source voltage is connected to a connecting point to a terminal for said first potential wherein, while a control signal is active, said first potential is applied to said clamping circuit and while said control signal is inactive, said first potential is applied to an amplifying section.

9. The voltage amplification circuit according to Claim 5, wherein a transistor for controlling supply of a source voltage is connected to a connecting point to a terminal for said first potential wherein, while a control signal is active, said first potential is applied to said clamping circuit and while said control signal is inactive, said first potential is applied to an amplifying section.